HIGH –K DIELECTRIC MATERIAL FOR CMOS DEVICES

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ABSTRACT: The scaling of MOSFET based on Moore's law will improve and enhance the performance of the device. This scaling requires the replacement of the conventional silicon oxide layer by high k- dielectric material having the higher permittivity. This high K-dielectric material will improve the band structure, conductivity and dielectric constant. The abintio calculations were carried on hf doped TiO2 high k dielectric material which will improve the above properties. The Band structure, Dielectric constant for different doping concentrations were obtained and analyzed.

Key words: Scaling, High-k, Material oxides

1. INTRODUCTION:

The fundamental building blocks for all computer chips—transistors—have tracked with Moore's Law for forty years. The transistors manufactured today are 25 times faster than and occupy less than 1% of the area of those builds four decades ago. In the past four decades the downsizing /scaling of MOSFET results to smaller device in smaller area, consumption of less power, and decrease in cost per transistor per function cost of integrated circuit.

1.1 SCALING ISSUES OF CMOS CIRCUITS:

The constraint for knowledge to scale assert that the finished manipulation consumption each constituent span stays steady that way that as density of the circuitry in a knowledge increases, the number of cooling necessity for the route stays

constant- if this was allowed to rise afterward a little point, the route should melts [1]. Countless limitations for the down scaling have been counseled in the works [1,3] Table1. Unfortunately the thickness gate silicon dioxide reaches its thinnest limit. Nowadays more scaling oxide layer is not capable to uphold insulating property, as manage tunneling dominates the leakage present more down scaling leads countless physical and technical limitations.

1.2 SCALING LIMIT OF SIO₂

Thirty years ago oxide thickness was 100 nm and nowadays it is 0.7 nm in creation as manage tunneling check of conventional oxide (SiO2) was 3 nm. The gate oxide up to 0.7 A° has been obtained possessing merely two atomic layer of SiO2. More Scaling is tough [10]. One of the most convincing examination

that clarified that 3 nm is frank check [11,15]. Employing the scanning transmission electron

microscope (STEM) probes and across detailed Electron Defeat Spectroscopy (EELS) measurements they learned that mechanism construction and chemical constitution of the oxide layer as slender as 0.7-1.2 nm. In the works work, the innate power gap was given by separation amid highest inhabit and lowest inhabited states. They discovered that to safeguard bulk like bonding for monolayer minimum three or four monolayer of SiO2 were needed. This is the early physical dimension of atomic level. EELS display that the SiO2 thickness have to have two layers to display a maximum gap of 8.9 eV [11]. The insufficient unsalable parameter interface thickness and mislead cross serving trials gate dielectric reliability. After oxide is in nanometer even tiny non-uniformity whichever in chemical constitution or even at external variation mechanism characteristics 10 crease [12,16] . As scaling plummet below two main groups elevated presentation (HP) mechanisms and low presentation (LP) devices. Electron Defeat Spectroscopy (EELS) measurements they learned that mechanism construction and chemical constitution of the oxide layer as slender as 0.7-1.2 nm. In the works work, the innate power gap was given by separation amid highest inhabit and lowest inhabited states. They discovered that to safeguard bulk like bonding for monolayer minimum three or four monolayer of SiO2 were needed. This is the early physical dimension of atomic level. EELS display that the SiO2 thickness have to have two layers to display a maximum gap of 8.9 eV [11]. The insufficient unsalable parameter interface thickness and mislead cross serving trials gate dielectric reliability. After oxide is in nanometer even tiny non-uniformity whichever in chemical constitution or even at external variation mechanism characteristics 10 crease [12,16] . As scaling plummet below two main groups elevated presentation (HP) mechanisms and low presentation (LP) devices.

2. ALTERNATE DIELECTRIC MATERIAL:

The choice of thicker class of materials, recognized as "high-k," could substitute today's silicon dioxide knowledge not for 45 nm or 32 nm but can additionally be scaled to the end-of-the roadmap knowledge nodes. Normally for high-k materials below investigation are Al2O3[22-26], ZrO2[27-29], HfO2[30], Ta2O5, TiO2[31-33], Er2O3, La2O3, Pr2O3, Gd2O3[34], Y2O3, CeO2 etc. and a little of their silicates such as ZrxSi1-xOy, HfxSi1-xOy, AlxZr1-xO2 etc.

3. Computational Method:

The abintio were calculations were carried out using the CASTEP a DFT based simulation software. The TiO₂ material of anatase were chosen for its better properties and it is doped with Hf which will improve the properties like dielectric constant at different doping concentration.

1.Band structure:

The Band Structure were shown in below figures. Band structure of these material increases with the doping concentration of Hf. The results shows the material band gap decreases which results in increase in the conductance of the material.

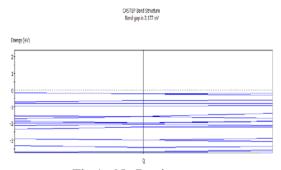


Fig 1: No Doping

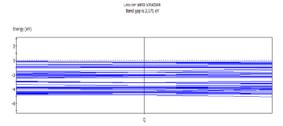


Fig 2:1% doping

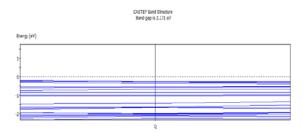
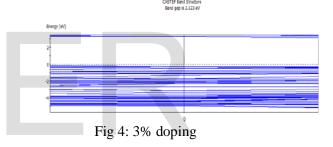


Fig 3: 2% Doping



2.Dielecric Constant:

Dielectric constant increases with the increase in the concentration of Hf thus with this it is used for the application in microelectronics

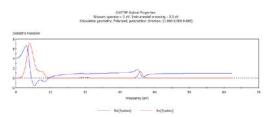


Fig 5: 0%doping

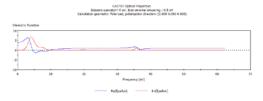


Fig 6: 1%doping

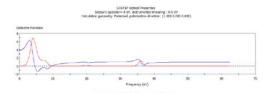


Fig 7: 2% doping

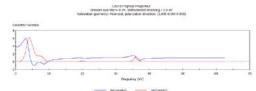


Fig 8: 3% Doping

Table 1. showing the list of rapidly expanding material in CMOS

Doping	Band	Dielectric
Concentration	Gap	Constant
0	2.177	6.9
10	2.171	6.1
20	2.171	7.6
30	2.123	5.5

The above table gives the band gap and dielectric constant values for different concentrations of doping. For 20 percent doping concentration the band gap is slightly reduced which leads improve the conductivity and dielectric constant.

4.CONCLUSION:

The high k dielectric material having high dielectric constant will improve the performance of the cmos, the doping of high k dielectric material to the TiO₂ material of anatase type will slightly reduce the bandgap which will enhance the better conductivity. This can also improve the dielectric constant of the material.

REFERENCES:

- [1] D.Rathee, et al, proc. Of National Conference ITM, oct6(2007)82-87
- [2] G.Moore, IEDM Tech., Dig. (1975)
- [3] H.Iwai, Hei Wong, Microelectronics Engg. 83(2006) 1867-1904
- [4] http://www.itrs.net

- [5] B. Doris, et al, IEDM Tech Dig. (2002) 267.
- [6] H.S.P Wong, et al, Proc. IEEE 87 (1999) 537
- [7] D.Frenk, et al, Proc. IEEE 89 (2001) 259.
- [8] H.Iwai Microelectronics Engg. 86(2009), 1520-1528.
- [9] Sidda Reddy Kurakulla, M.S in Engg. Thesis, IIS Banglore, oct 27, 2007.
- [10] ITRS 2003, Edition, Semiconductor Industry Association (SIA), Austin, SEMATECH USA, 2706
- [11] from :http://www.itrs.net/ntrs/publntrs.nsf
- [12] R Chau, et al, IEEE Electron Device Letter, 25 (2004) 408
- [13] D.Mullar, et al, Nature, 758(1999) 399
- [14] M. Radder, et al, IEDM technical Digest, (1998) 623.
- [15] H.Iwai, Hei Wong, Microelectronics Engg. 83(2006) 1867-1904.
- [16] H.Iwai, Sc in IEDM,2008.
- [17] H. Wong, V. A. Gitsenko, Microelectron. Reliab 42 (2002) 597.
- [18] K.Tse, et al, Microelectron Engg. 84(2007)2028.
- [19] S.H.Lo, et al, IEEE Electron devices lett. 18 (1997) 209.
- [19] G.D. Wick, et al, J. of App. Phy 89 (2001) 5243
- [20] D.Buchanan, IBM J.Res Develop 43(1999) 245
- [21] L.Manchanda, et al, Idem Technical Digest (1998) 605.
- [22] E.P.Gusev, et al, Appl. Phy lett 76(2000) 176.
- [23] M.Copel, et al, Appl. Phy lett 78(2001)2670.
- [24] D.A. Buchanan, et al, IEDM technical digest (2000)
- [25] R.Ludeka, et al, Appl. Phy lett 76 (2001)2886
- [26] M.Coepl, et al, Appl. Phy lett 76(2000)436
- [27] T.S.Jeon, et al, Appl. Phy lett 78(2001)368
- [28] W.J, et al, Appl. Phy lett 77(2000)3269.
- [29] L. kang, et al, IEDM technical Digest (2000)181
- [30] T.Modes, et al, Surf and coat Tech, 200 (2005)306
- [31] Sin-iti Kitazawa, et al, Thin Solid Films 515 (2006) 1901.
- [32] S.Murugesan, et al, Surf and Coat Tech, 201 (2007) 7713
- [33] Shoujing, et al, journal of physics series, 152 (2009) 012004
- [34] D. Buchanan, IBM J.Res\Develop 43(1999)245
- [35] A.M. Stoneham, Journal of Non-crystlline Solids 303 (2002) 114-122
- [36] Sin-iti Kitazawa, et al, Thin Solid Films 515 (2006) 1901
- [37] D. Buchanan, IBM J.Res\Develop 43(1999)245
- [38] C.Kittel, Introduction to solid state physics 7th edition, john wiely & sons Inc New York (1996)
- [39] G.D. Wilk, et al, J Appl Phy 89 (2001) 5243
- [40] J.Rebertson, J Vac Sci B 18 (2000) 1785
- [41] K Hubbard, D Sehlon, J Matr Reg 11 (1996) 2757
- [42] Ep Gusev, et al, Appl phy letter 76 (2000) 176
- [43] G.Lucovsky, et al, springer US (2002) 189.
- [44] T.Modes, et al, Surf and coat Tech, 200 (2005)306
- [45] Sin-iti Kitazawa, et al, Thin Solid Films 515 (2006) 1901.
- [46] S.Murugesan, et al, Surf and Coat Tech, 201 (2007) 7713
- [47] E.K.Evangelou, et al, J Appl phy 94 (2003) 318
- [48] E.P.Gusev, et al, IBM research, Microelectronics engg.,59 (2001) 341
- [49] Anieszka Borkowska, et al, workshop —Photnic and Microsystem || IEEE (2006).
- [50] K.F. Albertin, et al, Journal of circuits and system v2n2 (2007) 89-